further radiation hardening (and noise isolation), but at the cost of additional process steps.

It is contemplated that the buffered finFET devices disclosed herein may be used to form an SEU-resistant memory cell. It is also contemplated that the buffered finFET devices disclosed herein may be utilized to form noise-resistant analog circuits. The buffered finFET devices disclosed herein may also be used in other electronic circuits. Various types of integrated circuits, including field programmable gate arrays (FPGAs), microprocessors, application specific integrated circuits (ASICs), and so on, may utilize the buffered finFET devices disclosed herein.

FIG. **10** is a simplified partial block diagram of an FPGA **1000** that can include aspects of the present invention. For example, CRAM cells and/or analog circuits in the FPGA **1000** may be formed using the buffered finFET devices described herein. During operation of the FPGA, the CRAM cells store the configuration data which is used to program the FPGA. The analog circuits may be employed, for example, for high-speed serial communication links or for other purposes.

It is to be understood that FPGA **900** is described herein for illustrative purposes only and that the present invention can be implemented in many different types of integrated circuits. In other words, it should be understood that embodiments of the present invention can be used in numerous types of integrated circuits such as field programmable gate arrays (FPGAs), programmable logic devices (PLDs), complex programmable logic devices (CPLDs), programmable logic arrays (PLAs), digital signal processors (DSPs), microprocessors, and application specific integrated circuits (ASICs).

FPGA **1000** includes within its "core" a two-dimensional array of programmable logic array blocks (or LABs) **1002** that are interconnected by a network of column and row interconnect conductors of varying length and speed. LABs **1002** include multiple (e.g., ten) logic elements (or LEs).

An LE is a programmable logic block that provides for efficient implementation of user defined logic functions. An FPGA has numerous logic elements that can be configured to implement various combinatorial and sequential functions. The logic elements have access to a programmable interconnect structure. The programmable interconnect structure can be programmed to interconnect the logic elements in almost any desired configuration.

FPGA **1000** may also include a distributed memory structure including random access memory (RAM) blocks of varying sizes provided throughout the array. The RAM blocks include, for example, blocks **1004**, blocks **1006**, and block **1008**. These memory blocks can also include shift registers and FIFO buffers.

FPGA **1000** may further include digital signal processing (DSP) blocks **1010** that can implement, for example, multipliers with add or subtract features. Input/output elements (IOEs) **1012** located, in this example, around the periphery of the chip support numerous single-ended and differential input/output standards. Each IOE **1012** may be coupled to an external terminal (i.e., a pin) of FPGA **1000**.

Note that while the device structures shown in FIGS. **6** and **9** include p-n junctions which cover the entire horizontal cross section of the vertical fin-shaped structures. It is contemplated that other embodiments may form a p-n junction which only partially cover the horizontal cross section of the vertical fin-shaped structure. An example of such an embodiment is depicted in FIG. **11**.

The device in FIG. **11** differs from the device in FIG. **6** in that the buffer region **304** in FIG. **11** partially covers the horizontal cross section of the vertical fin-shaped structure. The uncovered portions **1102** of the horizontal cross section may be undoped or lightly doped semiconductor. This is shown in the C-C' cross section.

In the above description, numerous specific details are given to provide a thorough understanding of embodiments of the invention. However, the above description of illustrated embodiments of the invention is not intended to be exhaustive or to limit the invention to the precise forms disclosed. One skilled in the relevant art will recognize that the invention can be practiced without one or more of the specific details, or with other methods, components, etc.

In other instances, well-known structures or operations are not shown or described in detail to avoid obscuring aspects of the invention. While specific embodiments of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize. These modifications may be made to the invention in light of the above detailed description.

What is claimed is:

1. A transistor device comprising:
- a semiconductor substrate;
- a buffered vertical fin-shaped structure formed in the semiconductor substrate, the vertical fin-shaped structure including
  - an upper semiconductor layer including a channel region in between drain and source regions,
  - a buffer region beneath the upper semiconductor layer, the buffer region having a first doping polarity,
  - at least part of a well region having a second doping polarity which is opposite to the first doping polarity, and
  - at least one p-n junction between the buffer region and the well region which at least partially covers a horizontal cross section of the vertical fin-shaped structure; and
- a gate stack formed over the channel region of the upper semiconductor layer,
- wherein a first layer of the well region is directly above the buffer region, and a second layer of the well region is directly below the buffer region at the base of the buffered vertical fin-shaped structure, such that two p-n junctions are present between the buffer region and the well region.

2. The device of claim **1**, further comprising:
- oxide-filled trenches adjacent to the vertical fin-shaped structure.

3. The device of claim **2**, further comprising:
- an epitaxially-grown layer on the source and drain regions.

4. The device of claim **3**, further comprising:
- gate stack spacers adjacent to the gate stack,
- wherein the gate stack spacers electrically isolate a gate electrode of the gate stack from the source and drain regions.

5. The device of claim **1**, wherein the buffer region is directly above the well region such that one p-n junction is between the buffer region and the well region.

6. The device of claim **1**, further comprising:
- a well tap which bypasses the buffered vertical fin-shaped structure and electrically connects to the well region.

7. The device of claim **1**, wherein the horizontal cross section of the vertical fin-shaped structure is fully covered by the p-n junction.

8. A method of fabricating a finFET device comprising a buffered vertical fin-shaped structure on a semiconductor substrate, the method comprising: